with phosphorus in this step. However, the P type conductivity thereof can be maintained and is not reversed to the N type conductivity if they are doped with boron in a higher concentration in the previous step. --

A1 end

Please replace paragraph [0138] with the following

-- [0138] The structure in Fig. 8D is a mode of a pixel matrix circuit. In the structure of Fig. 8D, LDD regions 809 and 810 are provided on either the side closer to the source region or the side closer to the drain region. In other words, no LDD region is provided between two channel formation regions 811 and 812 and the gate wiring layers 808a and 808b. --

A2

Please replace paragraph [0146] with the following

-- [0146] The structure of this embodiment may also be applied to a pixel matrix circuit. The pixel matrix circuit in Fig. 9B uses a single layer of tantalum film for a gate wiring line and employs the above cladding structure, i.e., laminate 902, first conductive layer 902a and second conductive layer 902b, for a part of the gate wiring line that is required to reduce wiring line resistance (a part of the gate wiring line that does not function as a gate electrode). --

A3

REMARKS

The Examiner's Office Action dated July 31, 2002 has been received and its contents carefully noted. Applicants respectfully submit that this response is timely filed (with a one month Petition for Extension of Time) and is fully responsive to the Office Action. Accordingly, claims 1-18 remain pending, and are believed to be in condition for allowance for at least the following reasons.

With regard to the Examiner's objections to the specification and drawings, the Applicants submit a substitute specification, pursuant to 37 C.F.R. 1.125, with